CLAIMS

1. An apparatus for carrying out a measurement process for measuring a delay through a signal path within an integrated circuit (IC), the apparatus comprising:

a strobe generator,

for receiving an OSC signal that may be either logically true or logically false, for receiving TUNE data, and for receiving a STROBE signal,

for generating a signal A and a signal B when the OSC signal is logically false, each having an edge produced in delayed response to an edge of a STROBE signal supplied as input to the strobe generator, wherein the strobe generator provides a fixed delay between the STROBE signal edge and the signal A edge and provides a variable delay between the STROBE signal edge and the signal B edge, and wherein the variable delay is selected by TUNE data supplied as input to the strobe generator, and

for generating an OSCOUT signal when the OSC signal is logically true, wherein the OSC output signal has a period that is proportional to the variable delay selected by the TUNE data; and

a path probe implemented on the IC

for receiving, a TEST signal and a CAL signal that may be either logically true or logically false,

for generating a signal C at the signal path input in response to signal A when the TEST signal is logically true such that the signal path produces a signal D at its output, wherein each of signals C and D change state in response to each signal A edge;

for receiving signals B and D;

for responding to each signal B edge when the CAL signal is logically true by generating at least one indicating signal indicating whether signal C changed state before the path probe received the signal B edge, and

for responding to each signal, B edge when the CAL signal is logically false by generating said least one indicating signal indicating whether signal D changed state before or after the path probe received the signal B edge.

2. The apparatus in accordance with claim 1 wherein the strobe generator is implemented within the IC.

3. The apparatus in accordance with claim 1 further comprising a control circuit for supplying the STROBE signal and

TUNE data as inputs to the strobe generator, for supplying the CAL signal as input to the path probe, and for monitoring the indicating signal generated by the path probe.

4. The apparatus in accordance with claim 3 wherein the control circuit is implemented within the IC.

5. The apparatus in accordance with claim 3

wherein during a first phase of the measurement process, the control circuit sets the OSC signal logically false, sets the CAL signal logically true, and then executes a plurality of iterations of a process in which during each iteration of the process, it adjusts the TUNE data, sends a STROBE signal
edge to the strobe generator, and then monitors the indicating signal produced by the path probe, wherein the control circuit sets the TUNE data so that the strobe generator generates signal B edges with a different delay there between during each iteration of the process, until a pattern of successive indicating signal states indicates the TUNE data has reached a first setting for which the path probe circuit has receives the C and B edges nearly concurrently.

wherein during a second phase of the measurement process, the control circuit sets the OSC signal TRUE so that the strobe generator generates the OSCOUT signal having a period that is proportional to the variable delay selected by the TUNE data at the first setting,

wherein during a third phase of the measurement process, the control circuit sets the OSC signal logically false, sets the CAL signal logically false, and then executes a plurality of process iterations during each of which it adjusts the TUNE data, sends a STROBE signal edge to the strobe

generator, and then monitors the indicating signal produced by the path probe,

wherein the control circuit sets the TUNE data so that the strobe generator generates signal B edges with a different delay there between during each iteration of the process, until a pattern of successive indicating signal states indicates the TUNE data has reached a second setting for which the path probe circuit has receives the D and B edges nearly concurrently, and

wherein during a fourth phase of the measurement process, the control circuit sets the OSC signal TRUE so that the strobe generator generates the OSCOUT signal having a period that is proportional to the variable delay selected by the TUNE data at the second setting,

6. The apparatus in accordance with claim 5 further comprising a measurement circuit for monitoring the OSCOUT signal during the second and fourth phases of the measurement process to determine a path delay between edges of signals C and D.

7. The apparatus in accordance with claim 6 wherein the measurement circuit generates output data representing a difference between the period of the OSCOUT signal during the fourth phase of the measurement process, and the period of the OSCOUT signal during the second phase of the measurement process.

8. The apparatus in accordance with claim 6 wherein the measurement circuit generates output data representing a difference between a first number of cycles of a reference clock signal that occur during K cycles of the OSCOUT signal during the fourth phase of the measurement process, and a second number of cycle of the reference clock signal that occur during K cycles of the OSCOUT signal during the second phase of the measurement process, where K is an integer greater than 1.

9. The apparatus in accordance with claim 8 wherein the measurement circuit comprises:

a first counter for receiving the OSCOUT signal and for setting a GATE signal logically true for K cycles of the OSCOUT signal, and thereafter setting the GATE signal logically false; and

a second counter for counting cycles of the reference clock signal occurring only while the GATE signal is logically true, and for generating the output data indicating its current count,

wherein for the second phase of the measurement process, the second counter initially sets its output count to a value 0 and then increments the output count during each cycle of the reference clock signal while the GATE signal is logically true to produce a count having a first value when the GATE signal is subsequently set logically false, such that the first value is proportional to the variable delay selected by the TUNE data at the first setting, and

wherein for the fourth phase of the measurement process, the second counter initially sets its output count to a value that is less than 0 by the amount of the first value and then increments the output count during each cycle of the reference clock signal while the GATE signal is logically true to produce a count having a second value when the GATE signal is subsequently set logically false, such that the second value is proportional to a difference between the variable delays selected by the TUNE data at the second and first settings.

10. The apparatus in accordance with claim 9 further comprising a circuit for receiving the count generated by the second counter and for generating pass/fail data indicating whether the count is of a value residing within a predetermined range.

11. The apparatus in accordance with claim 2 wherein the strobe generator comprises:

a tapped delay line having an input and a plurality of taps, for delivering any signal appearing at its input to each of its taps with a different delay;

means for generating signal A in response to a signal appearing at one of the taps;

a first multiplexer controlled by the TUNE data for generating signal B in response to a signal appearing at any selected one of the taps, and

a second multiplexer controlled by the OSC signal for selectively delivering either the STROBE signal or signal B as input to the tapped delay line.

12. The apparatus in accordance with claim 1 wherein the path probe comprises:

a logic gate having a control input for receiving signal B, a data input, and a data output for producing the indicating signal, such that the indicating signal is of a logic state that indicates a logic state of a signal at the data input when a B signal edge last arrived at the clock input, and

a first multiplexer controlled by the CAL signal for selectively coupling either the C or D signal to the data input of the first logic gate.

13. The apparatus in accordance with claim 1 wherein the TUNE data also controls whether signal A changes to a state that matches or is opposite to a state of the STROBE signal during each signal A edge.

14. The apparatus in accordance with claim 10 wherein the strobe generator comprises:

a tapped delay line having an input and a plurality of taps, for delivering any signal appearing at its input to each of its taps with a different delay;

means for generating signal A in response to a signal appearing at one of the taps;

a first multiplexer controlled by the TUNE data for generating signal B in response to a signal appearing at any selected one of the taps, and

a second multiplexer controlled by the OSC signal for selectively delivering either the STROBE signal or signal B as input to the tapped delay line.

15. The apparatus in accordance with claim 14 wherein the path probe comprises:

a gate having a control input for receiving signal B, a data input, and a data output for producing the indicating signal, such that the indicating signal is of a logic state that indicates a logic state of a signal at the data input when a B signal edge last arrived at the clock input, and

a first multiplexer controlled by the CAL signal for selectively coupling either the C or D signal to the data input of the first logic gate.

16. The apparatus in accordance with claim 15 wherein the TUNE data also controls whether the signal A edge generated in response to each rising STROBE signal edge is a rising or falling signal edge.

17. The apparatus in accordance with claim 11 wherein the strobe generator further comprises:

a variable capacitor providing an amount of capacitance at the linked delay line selected by the TUNE data.

18. A method for measuring rising and falling edge path delays between an input and output of a signal path within an IC of the type which produces an output signal D at its output having edges in delayed response to an input signal C at its input, the method comprises:

a. forming a path probe within the IC proximate to the signal path and connected to the signal path's input and output wherein the path probe supplies the signal C to the signal path input in response to an input signal A, and monitors the signal D produced at the signal path output;

b. generating and supplying signal A and a signal B to the path probe, wherein signals A and B have edges generated in response to edges of a STROBE signal, wherein a STROBE-to-A edge delay is constant and a STROBE-to-B edge delay is variable,

c. adjusting the STROBE-to-B edge delay to a first delay for which the path probe receives signal B edges and generates signal C edges nearly concurrently

d. producing a first periodic signal having a period proportional to the first delay;

e. adjusting the STROBE-to-B edge delay to a second delay for which the path probe receives signal B edges and signal D edges nearly concurrently;

f. producing a second periodic signal having a period proportional to the second delay; and

g. processing the first and second periodic signals to determine the path delay through the signal path.

19. The method in accordance with claim 18 wherein step g comprises the substeps of:

g1. generating a first count of a number of cycles of a reference clock that occur during a predetermined number of cycles of the first periodic signal;

g2. generating a number indicating a number of cycles of the reference clock that occurring during predetermined number of cycles of the second periodic signal and the first count.

20. An apparatus for carrying out a measurement process for measuring delay through a plurality of signal paths within an integrated circuit (IC), the apparatus comprising:

a strobe generator implemented within the IC, for receiving an OSC signal that may be either logically true or logically false, for receiving TUNE data, and for receiving a STROBE signal, for generating a signal A and a signal B when the OSC signal is logically false, each having an edge produced in delayed response to an edge of a STROBE signal supplied as input to the strobe generator, wherein the strobe generator provides a fixed delay between the STROBE signal edge and the signal A edge and provides a variable delay between the STROBE signal edge and the signal B edge, and wherein the variable delay is selected by TUNE data supplied as input to the strobe generator, and for generating an OSCOUT signal when the OSC signal is logically true, wherein the OSC output signal has a period that is proportional to the variable delay selected by the TUNE data; and

a plurality of path probes implemented on the IC, each positioned proximate to a separate one of the signal paths, for receiving a TEST signal and a CAL signal that may be either

logically true or logically false, for generating a signal C at its corresponding signal path input in response to signal A when the TEST signal is logically true such that the signal path produces a signal D at its output, wherein each of signals C and D change state in response to each signal A edge, for receiving signal B from the strobe generator and the signal D at its corresponding signal path output, for responding to each signal B edge when the CAL signal is logically true by generating at least one indicating signal indicating whether the signal C it supplies to its corresponding signal path changed state before the path probe received the signal B edge, and for responding to each signal B edge when the CAL signal is logically false by generating said least one indicating signal indicating whether the signal D appearing at its corresponding signal path output changed state before or after the path probe received the signal B edge.

21. The apparatus in accordance with claim 21 further comprising a control circuit implemented within the IC for supplying the STROBE signal and TUNE data as inputs to the strobe generator, for supplying the CAL signal as input to the path probes, and for monitoring indicating signals generated by the path probes.

22. The apparatus in accordance with claim 21

wherein during a first phase of the measurement process, the control circuit sets the OSC signal logically false, sets the CAL signal logically true, and then executes a plurality of iterations of a process in which during each iteration of the process, it adjusts the TUNE data, sends a STROBE signal edge to the strobe generator, and then monitors the indicating signals produced by the path probes, wherein the control circuit sets the TUNE data so that the strobe generator generates signal B edges with a different delay there between during each iteration of the process, until a pattern of successive indicating signal states indicates the TUNE data has reached a first setting for which at least one of the path probe circuits has received the C and B edges nearly concurrently.

wherein during a second phase of the measurement process, the control circuit sets the OSC signal TRUE so that the strobe generator generates the OSCOUT signal having a period that is proportional to the variable delay selected by the TUNE data at the first setting,

wherein during a third phase of the measurement process, the control circuit sets the OSC signal logically false, sets the CAL signal logically false, and then executes a plurality of process iterations during each of which it adjusts the TUNE data, sends a STROBE signal edge to the strobe generator, and then monitors the indicating signals produced by the path probes, wherein the control circuit sets the TUNE data so that the strobe generator generates signal B edges with a different delay there between during each iteration of the process, until a pattern of successive indicating signal states indicates the TUNE data has reached a second setting for which at least
one of the path probe circuits has received the D and B edges nearly concurrently, and

wherein during a fourth phase of the measurement process, the control circuit sets the OSC signal TRUE so that the strobe generator generates the OSCOUT signal having a

period that is proportional to the variable delay selected by the TUNE data at the second setting,

23. The apparatus in accordance with claim 22 further comprising a measurement circuit for monitoring the OSCOUT signal during the second and fourth phases of the measurement process to determine a path delay between edges of signals C and D,

wherein the measurement circuit generates output data representing a difference between a first number of cycles of a reference clock signal that occur during K cycles of the OSCOUT signal during the fourth phase of the measurement process, and a second number of cycle of the reference clock signal that occur during K cycles of the OSCOUT signal during the second phase of the measurement process, where K is an integer greater than 1.

24. The apparatus in accordance with claim 23 wherein the strobe generator comprises:

a tapped delay line having an input and a plurality of taps, for delivering any signal appearing at its input to each of its taps with a different delay;

means for generating signal A in response to a signal appearing at one of the taps;

a first multiplexer controlled by the TUNE data for generating signal B in response to a signal appearing at any selected one of the taps, and

a second multiplexer controlled by the OSC signal for selectively delivering either the STROBE signal or signal B as input to the tapped delay line.

25. The apparatus in accordance with claim 23 wherein the path probe comprises:

a logic gate having a control input for receiving signal B, a data input, and a data output for producing the indicating signal, such that the indicating signal is of a logic state that indicates a logic state of a signal at the

data input when a B signal edge last arrived at the clock input, and

a first multiplexer controlled by the CAL signal for selectively coupling either the C or D signal to the data input of the first logic gate.

26. The apparatus in accordance with claim 21 wherein the TUNE data also controls whether signal A changes to a state that matches or is opposite to a state of the STROBE signal during each signal A edge.

27. A method for determining whether all path delays through a plurality of signal paths within an IC are within a predetermined range, whether each signal path is of the type which produces an output signal D at its output having edges in delayed response to a signal C at its input, the method comprises:

a. forming a plurality of path probes within the IC each proximate to a separate one of the signal paths and connected to the signal path's input and output wherein each path probe supplies a signal C to its corresponding signal path's input in response to a signal A, and monitors the signal D produced at the corresponding signal path's output;

b. generating and supplying signal A and a signal B in common to the path probes, wherein signals A and B have edges generated in response to edges of a STROBE signal, wherein a STROBE-to-A edge delay is constant and a STROBE-to-B edge delay is variable,

c. adjusting the STROBE-to-B edge delay to a first delay for which at least one of the path probes receives signal B edges and generates signal C edges nearly concurrently

d. producing a first periodic signal having a period proportional to the first delay;

e. adjusting the STROBE-to-B edge delay to a second delay for which at east one of the path probe receives signal B edges and signal D edges nearly concurrently;

f. producing a second periodic signal having a period proportional to the second delay; and

g. processing the first and second periodic signals to determine whether the path delays through all signal paths are within the predetermined range.

28. The method in accordance with claim 27 wherein step g comprises the substeps of:

g1. generating a first count of a number of cycles of a reference clock occurring during a predetermined number of cycles of the first periodic signal;

g2. generating a number indicating a number of cycles of the reference clock occurring during predetermined number of cycles of the second periodic signal and the first count.